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BEVER, HOFFMAN & HARMS, LLP
2099 GATEWAY PLACE
SUITE 320
SAN JOSE, CA 95110

EXAMINER	
LUU, CUONG V	

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte STEPHEN L. BADE, SHAY BEN-CHORIN, PAUL CAAMANO, MARCELO E. MONTOREANO, ANI TAGGU, FILIP C. THOEN, and DEAN C. WILLS

Appeal 2008-3432
Application 09/872,435[1]
Technology Center 2100

Decided:[2] March 20, 2009

Before JOHN C. MARTIN, JAY P. LUCAS, and CAROLYN D. THOMAS, *Administrative Patent Judges*.

LUCAS, *Administrative Patent Judge*.

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[1] Application filed June 1, 2001. Appellants claim the benefit under 35 U.S.C. § 119 of provisional applications 60/208,900, filed 06/2/2000 and 60/230,171 filed 09/1/2000. The real party in interest is Synopsys, Inc.

[2] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal from a final rejection of claims 37 to 72, 74 to 78, and 89 under authority of 35 U.S.C. § 134(a). The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

Appellants' invention relates to a computer method and system to simulate embedded systems under design. Embedded systems are hardware and software based components that form a building block in a larger system. The claimed system assists in the design of these embedded systems by allowing the designer to simulate different microprocessors and related other components in the design, and evaluate how, when programmed, they work and what their cost, performance and other attributes will be. In the words of the Appellants:

> An integrated design environment (IDE) is disclosed for forming virtual embedded systems. The IDE includes a design language for forming finite state machine models of hardware components that are coupled to simulators of processor cores, preferably instruction set accurate simulators. A software debugger interface permits a software application to be loaded and executed on the virtual embedded system. A virtual test bench may be coupled to the simulation to serve as a human-machine interface. In one embodiment, the IDE is provided as a web-based service for the evaluation, development, and procurement phases of an embedded system project. IP components, such as processor cores, may be evaluated using a virtual embedded system. In one embodiment, a virtual embedded system is used as an executable specification for the procurement of a good or service related to an embedded system.

(Abst. 133.)

Claim 37 and Claim 52 are exemplary:

37. In a computer system having a graphical interface (GUI) and a design language for forming a finite state machine (FSM) representation of a hardware partition of an embedded system, a method of designing an embedded system, the method comprising:

forming a library of processor cores including an instruction set accurate simulator for each of the processor cores in the library;

responsive to a first sequence of user commands, selecting at least one of the processor cores from the library as a target processor core;

responsive to a second sequence of user commands, forming a virtual embedded system including an instruction set accurate simulator of a target processor core and coupling read, write, and interrupt signals of the instruction set accurate simulator with an FSM simulation of at least one hardware element, wherein generating said FSM simulation comprises applying a design language having at least one graphical symbol and adapted to form a finite state machine representation of electronic hardware, each graphical symbol of the design language having a graphical portion and a user-definable textual portion defining the behavior of the graphical symbol;

responsive to a request from the user, loading an executable binary file of a software application compiled for the target processor;

executing a simulation of the virtual embedded system running the software application; and

responsive to a user request, displaying on the GUI a graphical representation of the execution of the software application on the virtual embedded system that includes a software debugger interface to debug the

loaded software and a virtual test-bench associated with the GUI and adapted to interact with the simulation, wherein the virtual test-bench is created using a test-bench builder for generating a graphical representation of at least one interactive test-bench and for selecting signals or variables associated with the FSM and to be coupled to a graphical representation of a user interface for each interactive test-bench, to emulate user input to and device output from the virtual embedded system.

52. A computer implemented method of embedded system design, the method comprising:

selecting an instruction set accurate simulator of a target processor core;

generating a virtual hardware component that is a finite state machine (FSM) representation of at least one hardware component, said generating comprising applying a design language having at least one graphical symbol and adapted to form an FSM representation of electronic hardware, each graphical symbol of the design language having a graphical portion and a user-definable textual portion defining the behavior of the graphical symbol;

linking read, write, and interrupt signals of the instruction set accurate simulator of the target processor core with corresponding signals of the at least one virtual hardware component to form a virtual embedded system;

creating a virtual test bench using a test bench builder for generating a graphical representation of at least one interactive test bench and for selecting signals or variables to be coupled to a graphical representation of a user interface for each interactive test bench;

coupling the virtual test bench to at least one signal or variable of the virtual embedded system to simulate a human/machine interface; and

coupling a software debugger to the virtual embedded system that is configured to load and run on the virtual embedded system at least one binary program executable of a software application compiled for the target processor core.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Rompaey	EP 0,772,140 A1	Jul. 05, 1997
Van Huben	US 6,094,654	Jul. 25, 2000
Hellestrand	US 6,263,301 B1	Jul. 17, 2001 (filed Jan. 26, 2000)
Schwab	US 2004/0250083 A1	Dec. 09, 2004 (filed May 01, 2001)
Schubert	US 2005/0193280 A1	Sep. 01, 2005 (filed Nov. 28, 2000)

Datasheet Interactive Simulation Library, Cadence Design Systems, (1997.)

REJECTIONS

The Examiner rejects the claims as follows:

R1: Claims 37 to 39 and 49 to 51 stand rejected under 35 U.S.C. § 103(a) for being obvious over Rompaey in view of Cadence and further in view of Hellestrand.

R2: Claims 40 to 42 stand rejected under 35 U.S.C. § 103(a) for being obvious over Rompaey in view of Cadence and Hellestrand and further in view of Schwab.

R3: Claims 43 to 48 stand rejected under 35 U.S.C. § 103(a) for being obvious over Rompaey in view of Cadence and Hellestrand and further in view of Van Huben.

R4: Claims 52 to 59, 64, and 89 stand rejected under 35 U.S.C. § 103(a) for being obvious over Rompaey in view of Cadence.

R5: Claims 60 to 63 stand rejected under 35 U.S.C. § 103(a) for being obvious over Rompaey in view of Van Huben.

R6: Claims 65 to 67 stand rejected under 35 U.S.C. § 103(a) for being obvious over Rompaey in view of Schubert.

R7: Claims 68 to 70 stand rejected under 35 U.S.C. § 103(a) for being obvious over Rompaey in view of Cadence and Van Huben.

R8: Claims 71 to 72 stand rejected under 35 U.S.C. § 103(a) for being obvious over Rompaey in view of Cadence and Van Huben and further in view of Schwab.

R9: Claims 74 and 76 to 78 stand rejected under 35 U.S.C. § 103(a) for being obvious over Rompaey in view of Van Huben and Cadence.

R10: Claim 75 stands rejected under 35 U.S.C. § 103(a) for being obvious over Rompaey in view of Van Huben, Cadence, and further in view of Schwab.

Groups of Claims:

Claims will be discussed in the order of the rejections, with the first claim in each rejection being representative, unless otherwise indicated. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Appellants contend that the claimed subject matter is not rendered obvious by Rompaey alone, or in combination with the other cited references, for failure of the references to teach certain claimed limitations. The Examiner contends that each of the claims is properly rejected.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Brief and Reply and the Answer for their respective details. Only those arguments actually made by Appellants have been considered in this opinion. Arguments which Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived.

We reverse the rejections.

ISSUE

The issue is whether Appellants have shown that the Examiner erred in rejecting the claims under 35 U.S.C. § 103(a). The issue turns on whether the references teach the method of designing an embedded system with the claimed features, most notably using a simulator with a Finite State Machine (FSM) simulation.

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

1. Appellants have invented a method of modeling the performance of computer systems under design, including various processor cores, related peripherals, software and connections, the modeling being useful in predicting the performance and cost characteristics of a proposed computer system. (Spec: 6-9). The hardware simulation is based on a Finite State Machine design, which give certain benefits of speed, implementation and cost. (Spec., ¶[0139]).

2. The reference Rompaey teaches a design environment for modeling the hardware and software aspects of a computer system. Using Rompaey, the designer first concentrated on the functionality of the modeled system, using what are called primitive channels, ports etc. (Col. 16, l. 25). Then using what are called hierarchical processes or channels the behavior of the primitive channels are refined to give more accurate results. (*Id.*).

PRINCIPLES OF LAW

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a

rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

The analysis begins with an interpretation of the claims: "Both anticipation under § 102 and obviousness under § 103 are two-step inquiries. The first step in both analyses is a proper construction of the claims . . . . The second step in the analyses requires a comparison of the properly construed claim to the prior art." *Medichem S.A. v. Rolabo S.L.*, 353 F.3d 928, 933 (Fed. Cir. 2003) (internal citations omitted).

ANALYSIS

From our review of the administrative record, we find that Examiner has presented a detailed discussion of the prima facie case for the rejections of Appellants' claims under 35 U.S.C. § 103. The prima facie case is presented on pages 3 to 21 of the Examiner's Answer. In opposition, Appellants present a number of arguments.

Arguments with respect to the rejection of claims 37 to 39 and 49 to 51 under 35 U.S.C. § 103 [R1]

Appellants contend that Examiner erred in rejecting claims 37 to 39 and 49 to 51 as the reference Rompaey does not teach or suggest forming a virtual embedded system that includes a Finite State Machine (FSM).

(Br:19, middle). Appellants point to the three sections in Rompaey in which the FSM is said to be taught, and explain how none of these citations teaches the FSM simulation as claimed. (*Id.*)

As this is a seminal issue in resolving this appeal, we will investigate this issue in detail. An FSM model is based on analyzing the transition of the modeled system or process as it transitions from one steady state to the next in response to triggering events. (*See* Spec., p. 52 *ff*). In performing the transitions the process executes actions which, based on calculations, change assigned values to variables. The progress of the model can be stopped at any particular state, and the variables analyzed to determine the condition and values of the modeled process or system. Appellants' Figure 11 demonstrates the various parts of an FSM model, including an Event Queue and a Time Queue, described at Spec, ¶[0133]. Appellants assert that an FSM allows an engineer to rapidly design a representation of a process on a hardware system with low simulation overhead in a fraction of the time as previously required, which helps in defining system architecture and other design tasks. (Spec: 57, middle).

The European patent reference Rompaey presents a design methodology and environment for modeling hardware and software simulations of computer systems, including the simulation of various processor cores (e.g., Intel 80, etc.). The Examiner asserts that the claimed limitation of forming a virtual embedded system using FSM modeling of the hardware elements is obvious over Rompaey as indicated in that reference in

column 9, in column 20 and 21, in column 11 and in Figure 11. (Ans.: 4, middle). We have studied the reference Rompaey at the cited sections, and indeed the entire reference in full, and do not find the relied upon teaching of an FSM model. Modeling in Rompaey is based on defining a series of primitive channels which lay out the basic connections of the system being modeled, followed by refinements written as what are called hierarchical channels to acquire more accurate performance results. (*See* FF#2 above). We note also that neither the Cadence nor the Hellestrand references teach the indicated FSM modeling. The Examiner responds to the Appellants' challenge to the reference by discussing the components for modeling a processor core, and reference again to column 9. (Ans.: 22, bottom), but without indicating an FSM based reference. We agree with the Appellants that this is not sufficient foundation to render the specific limitations in the claims obvious.

Reviewing the rejections R2 to R10 we note that Rompaey is relied upon in each rejection for the teaching of the FSM simulation of the hardware elements. We find that Rompaey does not provide that teaching, and the deficiency is not supplied by any of the other cited art. Reviewing the independent claims 37, 52, 64, 68, and 74, we note that each of the independent claims contains a limitation similar to the one in claim 37 concerning FSM modeling of critical components of the embedded hardware system.

We therefore find that each of the groups of references cited in the rejections R1 to R10 fails to render obvious the respective claims.

As this argument is dispositive of the rejections in this appeal, consideration of the other issues raised by the Appellants is deferred.

CONCLUSION OF LAW

Based on the findings of fact and analysis above, we conclude that the Examiner erred in rejecting claims 37 to 72, 74 to 78, and 89 [R1 to R10].

DECISION

The Examiner's rejections R1 to R10 of claims 37 to 72, 74 to 78, and 89 are Reversed.

REVERSED

rwk

BEVER, HOFFMAN & HARMS, LLP
2099 GATEWAY PLACE
SUITE 320
SAN JOSE CA 95110